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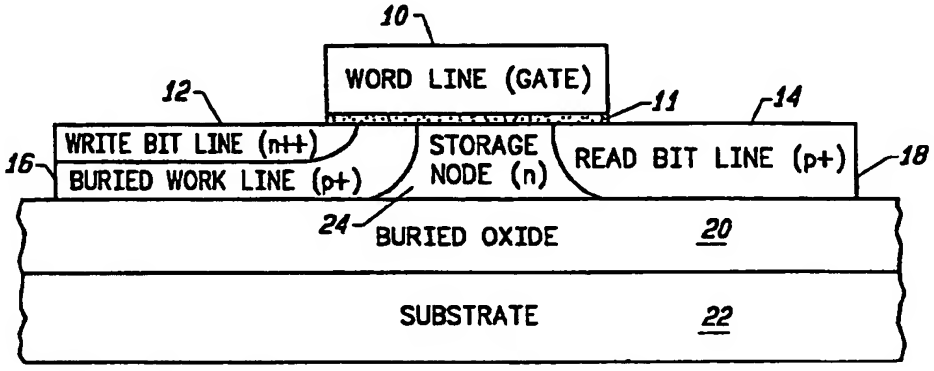

(57) Abstract

A DRAM device has a first semiconductor region (18) of one conductivity on the silicon film of a silicon-on-insulator substrate (22). A second (16) and a third (14) semiconductor region of the opposite conductivity are formed in the first semiconductor region (18). A fourth semiconductor region (12) of the same conductivity type as the first semiconductor region (18) is formed within the second semiconductor region (16) with higher doping concentration. A insulating layer (11) is formed on the semiconductor surface. On top of the insulating layer (11), a gate electrode (10) is formed and is at least partially overlapped with the first (18), the second (16), the third (14), and the fourth (12) semiconductor region. A storage node (24) is formed in the first semiconductor region (18) between the second (16) and the third (14) semiconductor region where the information is stored. The amount of charge stored in the storage node (24) is controlled by a first transistor including the fourth semiconductor region (12), the second semiconductor region (16), the storage node (24), and the gate electrode (10).

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A CAPACITORLESS DRAM DEVICE ON SILICON-ON-INSULATOR SUBSTRATE

BACKGROUND OF THE INVENTION

This invention relates generally to semiconductor devices, and more particularly the invention relates to dynamic random access memories (DRAM) and cell structures.

Dynamic random access memory (DRAM) is a major semiconductor product and has been the "technology driver" for the semiconductor industry. The commercial success of DRAM results from the smallness of the memory cell unit, which makes high storage density and low cost possible. DRAM cell contains one transistor for controlling READ/WRITE operations and one capacitor for charge storage. The transistor uses the smallest feature size transistor available thus drives the front-end technology such as lithography, transistor scaling and isolation. The technology developed for DRAM can later be used for fabricating other semiconductor products.

However the challenge of DRAM technology of 64 megabits and beyond has been more on how to build a large capacitor in a small area rather than on transistor scaling. The storage capacitor needs about 30fF to provide enough signal-to-noise ratio. Novel dielectric-constant material or novel memory cell structure become the main focuses for current DRAM technology . Besides the fact that the fabrication process of 64 megabits DRAM and beyond is becoming more and more difficult, the development and manufacturing cost is increasing tremendously yet the technology developed for DRAM is not extendible to other semiconductor products. The limit of C_S=30fF is not likely to be lessened if the principles of the cell operation, the charge-sharing between the storage capacitor and the READ (bit line) capacitor (i.e., the single-event upset READ scheme), remain unchanged, and will only become more stringent for gigabits DRAM technology.

The concept of "gain cell" has been proposed to alleviate the dependence on large cell capacitance. Many gain cells proposed use an additional transistor (e.g., JFET Complementary MOS , or BJT) to amplify the charge stored in a smaller capacitor whose size is lowerbounded by soft-error consideration

(~10fF). However these gain cells either take larger cell layout area or involve complicated fabrication process, both of which increase development and manufacturing costs. Another category of gain cells use the concept of "dynamic threshold ." These gain cells do not need large storage capacitors, however, gain cells based on the dynamic threshold operation are sensitive to the processing condition and maybe difficult to manufacture.

SUMMARY OF THE INVENTION

This invention provides a capacitorless DRAM device on silicon-on-insulator substrate with large read current, good immunity to α-particle-induced single-even-upset, and simple fabrication process. The size of the capacitorless DRAM device is that of a single transistor, which makes it very attractive for ultra high density memory applications. Using SOI substrate not only avoids many problems that make prior art devices impossible or impractical but also greatly simplifies the fabrication process. Since the capacitorless DRAM device employs the operation concept similar to dynamic threshold devices , the large capacitor is not needed. In the capacitorless DRAM the charge is stored in the front surface of the thin silicon film of silicon-on-insulator substrate. The stored charge modulate the function of the read transistor (e.g. the threshold voltage of a MOSFET). The amount of charge read in the capacitorless DRAM cell can easily exceed the amount of charge read in ordinary DRAM cell (~100fC).

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a cross section view of a capacitorless DRAM cell in accordance with one embodiment of the invention, and FIG. 1B is a schematic diagram of the DRAM cell.

FIG. 2 is an energy band diagram of the DRAM cell in a "0" storage state.

FIG. 3 is an energy band diagram of the DRAM cell during a write operation.

FIG. 4 is an energy band diagram of the DRAM cell with a "1" stored therein.

FIG. 5 is an energy band diagram of the DRAM cell during a read operation.

FIG. 6 is an energy band diagram where the DRAM cell is purged.

FIG. 7 illustrates transient RBL current of the DRAM cell during read/write cycles.

FIG. 8 illustrates read (RBL) current as a function of read (WL) voltage with and without stored electrons.

FIG. 9 is a plan view of an array of DRAM cells in accordance with an embodiment of the invention.

FIG. 10 is a schematic diagram of the array of DRAM cells of FIG. 9.

FIG. 11 is a schematic diagram of an alternative embodiment of the array of DRAM cells of FIG. 9.

FIG. 12 is a plan view of an array of DRAM cells in accordance with another embodiment of the invention.

FIG. 13 is a cross section view of the DRAM device array of FIG. 12 taken along a bit line, BL.

FIG. 14 is a schematic diagram of the DRAM device array of FIG. 12.

DETAILED DESCRIPTION OF THE ILLUSTRATIVE EMBODIMENT

In FIG. 1A the cross-sectional view of the capacitorless DRAM device, it has a word line (WL) formed by the gate 10 formed on gate insulator 11, an n++ write bit line (WBL) 12, a p+ read bit line (RBL) 14, and a p+ buried word line (BWL) 16. The device is formed in a semiconductor layer 18 on a first insulating layer 20 which insulates the device from the supporting substrate 22. The substrate and insulating layer can be integral and in a conventional silicon or sapphire structure. This device can also be realized by using the opposite conductivity type semiconductor in each region of FIG. 1. The write transistor is composed of WBL, BWL, the floating body, and the gate. The read transistor is composed of the RBL, the floating body, storage node 24, the BWL, and the gate (FIG. 1B). They are integrated together within one compact structure. Compared to ordinary DRAM cells, the fabrication process is simpler. Though the cross sectional view of the present invention looks similar to the device taught in U.S. Patent 4,395,723, they are different in important ways. In the present invention, node BWL that resembles the floating storage nodes 102 in FIG. 1A, 202 in FIG. 2A, 302 in FIG. 3A and 402 in FIG. 4A of U.S. Patent

4,395,723 is not the storage node. It is electrically connected to the peripheral circuit. In the present invention the storage node is the floating body that resembles nodes 104 in FIG. 1A, 204 in FIG. 2A, 304 in FIG. 3A, and 404 in FIG. 4A, which in US Patent 4,395,723 are biased at ground or V_{CC}. For the device taught in US Patent 4,395,723 the storage node is built on the substrate a region of the opposite conductivity type semiconductor. Therefore the substrate needs low doping concentration which results in high resistivity (104 in FIG. 1A, 204 in FIG. 2A, 304 in FIG. 3A, and 404 in FIG. 4A in US Patent 4,395,723), and the storage node needs high doping concentration which results in high junction capacitance (C_1 in FIG. 1A and similarly in FIGs. 2A, 3A, and 4A in US Patent 4,395,723). These are significant shortcomings which make the device taught in US. Patent 4,395,723 impractical. The transistor that provides the read current (e.g. 120 to 106 in FIG. 1A, 220 to 206 in FIG. 2A, 320 to 306 in FIG. 3A, and 420 to 406 in FIG. 4A in US. Patent 4,395,723) are vertical transistors (the source is situated below the drain) requiring the current to flow through the lightly doped, high-resistivity, region. This added resistance significantly reduces the available current in comparison with the conventional lateral transistors. In addition, the bit line of the memory (120 in FIG. 1A, 220 in FIG. 2A, 320 in FIG. 3A, and 420 in FIG. 4A in US. Patent 4,395,723) has large junction capacitance (C_1 in FIG. 1A and similarly in FIGs. 2A, 3A, and 4A in US. Patent 4,395,723) which further reduces the speed performance. A third shortcoming is the difficulty of routing the required negative voltages (Table 1 in US. Patent 4,395,723). Without silicon-on-insulator this would imply the use of a triple-well technology to isolate the devices carrying the negative voltage, resulting in more complex circuit design, larger chip size, lower performance, and higher cost. Finally α-particle induce single-event-upset is a problem because of the large storage node junction.

In the present invention the storage region is not formed on the substrate, but is the starting material itself. The present invention solves all these problems through the use of silicon-on-insulator substrate. On a silicon-on-insulator substrate the devices carry negative voltages can be isolated (by oxide, not by pn junctions) from those carrying positive voltages without special precautions. The immunity to α-particle-induced single-event-upset is improved because the junction area is reduced and the path from the charge generated by the α-particle to the storage node is cut off. Furthermore, normal lateral transistors with low resistivity source and drain are used for read and write, the magnitude of the read current will not be degraded. Also the read bit line capacitance is smaller because it is connected to the junction capacitance on

the lightly-doped substrate (between RBL and the floating body). Large read current and small bit line capacitance are important factors in determining DRAM performance.

In the first embodiment, the memory device is operated according to Table 1:

Node / Operation	WL	WBL	RBL	BWL	SUB
Purge	0	0.6	0	GROUND	GROUND
Read	0.6		0.6		
Hold	1.8				
Write "1"	3				
Write "0"		1.8			

TABLE. 1 An example of the operating voltages of the capacitorless DRAM device of accumulation mode.

The memory states "0" and "1" are distinguished by the amount of majority carriers injected from WBL into the storage node (accumulation mode operation), which is fundamentally different from the device proposed in U.S. Patent 4,395,723 in which the memory states of "0" and "1" are distinguished by the depletion of majority carrier out of the storage node (depletion mode operation). In this embodiment, when the capacitorless DRAM device is not performing read and write, i.e., in the holding state, the biasing voltages are: WL 1.8 V, RBL and WBL 0.6 V, and BWL 0 V. The positive WL voltage tends to accumulate the floating body. Since there is no electron supply to form the accumulation layer, a potential well is formed in the floating body (FIG. 2). In writing the capacitorless DRAM cell, WL voltage increases to 3 V. WBL is biased at 0.6 V for

writing a "1" and at 1.8 V (larger than 1.2 V will be enough) for writing a "0." With WL voltage at 3 V and WBL voltage at 0.6 V for writing a "1", the write NMOSFET is turned and electrons inject from WBL into the storage node to supply the accumulation layer at the front surface of the floating body until the potential well is "filled," that is, fermi levels of the WBL and of the front surface of the floating body are aligned (FIG. 3). The write time takes less than a few nano seconds. For writing a "0" WBL is biased at 1.8 V, electrons will be blocked by the barrier and the potential well remains empty (FIG. 3). After writing the capacitorless DRAM device, WL returns to the holding voltage 1.8 V (FIG. 2 and 4).

The write mechanism of the capacitorless DRAM device is not limited to the MOSFET operation as described in the example. Punchthrough and tunneling are also possible mechanisms that can be used for the write operation. For some capacitorless DRAM device array layout BWL voltages can also be used for write operations if BWLs are not common to the whole array but are laid out along the WL directions. In fact it is advantageous of using both WL and BWL for the write operation because less WL voltage such as 2.5 V is needed if BWL is biased at to 0.6 V during write.

For the read operation, WL is biased to 0.6V. The potential of the storage node is capacitively coupled to the WL voltage thus the hole barrier is reduced. If the capacitorless DRAM device is in state "1" with electrons in the front surface accumulation layer of the storage node, the read transistor will turn on when WL is 0.6 V and a large hole current will flow from RBL to BWL to generate a signal to be detected at RBL. If the capacitorless DRAM device is in state "0" with no electron in the front channel of the floating body, the read transistor will not turn on when WL is 0.6 V and there is no current flow from RBL to BL (FIG. 5). The operation of the read transistor can function either like a MOSFET or a BJT, depending on the device design. For example, when WL is biased at the read voltage, if the voltage coupling from WL to the floating body is strong such as in the case that the film is fully-depleted and that the band-bending of the floating body is large, the read transistor behaves more like an MOSFET and the read operation is non-destructive because the potential barrier for electrons residing in the front surface accumulation layer remains high even the hole barrier at the back surface is low. If the voltage coupling from WL to the floating body is weak as in the case the film is non-fully-depleted that the band-bending of the silicon film is small. part of the floating body will be quasi-neutral and the read transistor behaves like a BJT. The read

operation is destructive because the electron barrier in the front surface accumulation layer is low when the hole barrier is low. In this case the holes are not necessarily flowing through the back surface of the silicon-on-insulator film from RBL to BWL.

In this embodiment, the capacitorless DRAM device has to be in state "0" before it can be written again. One way to achieve this is to employ destructive read, then the capacitorless DRAM device is ready for writing after read. If the read operation is non-destructive, an optional purge operation can be employed. Purge can be done by applying 0 or negative voltage to WL to expel the electrons out of the potential well. Increasing BL voltage can also help the efficiency of purging the cell and avoid heavy turn-on of the read transistor (FIG. 6). The memory operation of the capacitorless DRAM device in the first embodiment is demonstrated in FIG. 7 and 8 by the numerical simulations.

In the second embodiment, the capacitorless DRAM cell can be operated in the depletion mode according to Table 2:

Node / Operation	WL	WBL	RBL	BWL	SUB
Read	-1.5	0	-1	GROUND	GROUND
Hold	0				
Write "1"	3				
Write "0"		2			

TABLE. 2 An example of the operating voltages of the capacitorless DRAM device of depletion mode.

For this embodiment the mode of operation is similar to the prior art device in US. Patent 4,395,723 but the storage node is different. In the holding state WL is biased at 0 V. In writing "0" WBL is biased at 2 V and WL is biased at 3 V to turn on the write NMOSFET so that the floating body is charged to 2 V to increase the threshold voltage of the read PMOSFET. In writing a "1" WBL is biased at 0 V and WL is biased at 3 V so that the floating body is charged to 0 V. For reading, WL is biased at -1.5 V

and RBL is biased at -1 V. The "0" and "1" states are thus distinguished with different threshold voltage of the read transistor. The read operation is non-destructive. This embodiment requires the voltage coupling from WL to BWL to be stronger than the voltage coupling from WL to the floating body. However BWL usually has a higher doping concentration therefore a weaker voltage coupling from WL. One way to increase voltage coupling from WL to BWL is to use thinner oxide in the region between WL and BWL.

In the embodiment of the memory array architecture, the capacitorless DRAM device described above can be put into a two-dimensional contactless array shown in FIG. 9. The schematic diagram is shown in FIG. 10. If BWLs are grounded at all times they can be contacted through metal or polysilicide interconnect parallel to WL once every several rows. To fully explore the high speed performance of the capacitorless DRAM devices, using two metal lines per memory array column (one for RBL and one for WBL) is desirable so that the RBL has low capacitance. In considering the memory density however it is desirable to use one metal line per column. Since the read and write operations of the capacitorless DRAM device are quite independent, that is, during the read operation, WBL can be a high impedance node, and vise versa. The concept of "alternative metal scheme" can possibly be employed by sharing RBL and WBL with one metal with switching transistors to achieve one metal line per bit. For example, before the write cycle starts, BWL is charged to 0V through select transistor S_2 and the metal line. Then S2 is turned off and S_1 is turned on so that metal line is connected to WBL to perform write. The read cycle can be done similarly.

An another embodiment which focuses on improving the array density of the capacitorless DRAM device is to use one metal bit line for both RBL and WBL. In this way the memory cell size can be reduced to $4(F+a)^2$, where F is the minimum feature size and a is the alignment tolerance. For example, FIG. 12, 13, and 14 are the array layout, the array cross section along BLs, and the array schematic diagram. The operating voltages of this embodiment is listed in Table 3 :

W/BL's / Functions	WL1 (selected)	BWL	RBL &WBL	WL2	Other WL's
HOLD	3	-1.5	0	1.5	3
READ "1"	0	-1.5	< 0		
READ "0"			0		
PURGE	-1.5	0	~ 0		
WRITE "1"	3	0	0		
WRITE "0"			0.6		

Table 3 Operating voltages for the capacitorless DRAM device with $4(F+a)^2$ unit cell size.

Since two neighboring WLs (WL1 and WL2 in FIG. 12 and 14) are sharing with one BWL, when WL1 in FIG. 12 is selected, WL2 has to be biased at 1.5 V to avoid data disturbance. The price paid for using one bit line for both RBL and WBL is that the read and write operations can not be optimized separately, and the bit line voltage swing is limited to about 0.6 V to avoid disturbing the data in memory devices in unselected rows.

While the invention has been described with reference to specific embodiments, the description is illustrative of the invention and is not to be construed as limiting the invention. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A capacitorless dynamic memory cell comprising

a body including a support substrate, a first insulating layer on said substrate, and a semiconductor layer on said first insulating layer, said semiconductor layer having a surface,

a storage node in said semiconductor layer abutting said surface, and electrically isolated from said substrate by said first insulating layer, said storage node having a net dopant concentration of a first conductivity type,

a write bit line region abutting said surface and spaced from said storage node, said write bit line region having a net dopant concentration of said first conductivity type,

a buried word line region abutting said surface and positioned between and abutting said storage node and said write bit line, said buried word line region having a net dopant concentration of a second conductivity type,

a read bit line region abutting said surface and said storage node opposite from said buried work line region, said read bit line region having a net dopant concentration of said second conductivity type,

a second insulating layer on said surface, and

a gate electrode on said second insulating layer positioned over said storage node and said buried word line region, said gate electrode functioning with said write bit line region, said buried word line region, and said storage node as a write transistor, and said gate electrode functioning with said buried work line region, said storage node, and said read bit line region as a read transistor.

2. The memory cell as defined by claim 1 wherein said first conductivity type is n- type and said second conductivity type is p- type.

3. The memory cell as defined by claim 2 wherein electrons from said buried word line region flow into said storage node in writing into said cell and increasing conductance of said read transistor.

4. The memory cell as defined by claim 2 wherein said storage node is charged with a positive voltage from said write bit line region in writing into said cell and increasing threshold voltage of said read transistor.

5. The memory cell as defined by claim 4 wherein said body comprises a silicon substrate with said first insulating layer comprising silicon oxide and said semiconductor layer comprising silicon.

6. The memory cell as defined by claim 1 wherein said body comprises a silicon substrate with said first insulating layer comprising silicon oxide and said semiconductor layer comprising silicon.

7. A dynamic random access memory comprising an array of memory cells arranged in rows and columns, each memory cell comprising

a body including a supporting substrate, a first insulating layer on said substrate, and a semiconductor layer on said first insulating layer, said semiconductor layer having a surface,

a storage node in said semiconductor layer abutting said surface and electrically isolated from said substrate by said first insulating layer, said storage node having a net dopant concentration of a first conductivity type,

a write bit line region abutting said surface and spaced from said storage node, said write bit line region having a net dopant concentration of said first conductivity type,

a buried word line region abutting said surface and positioned between and abutting said storage node and said write bit line, said buried work line region having a net dopant concentration of a second conductivity type,

a read bit line region abutting said surface and said storage node opposite from said buried work line region, said read bit line region having a net dopant concentration of said second conductivity type,

a second insulating layer on said surface, and

a gate electrode on said second insulating layer positioned over said storage node and said buried word line region, said gate electrode functioning with said write bit line region, said buried word line region, and said storage node as a write transistor, and said gate electrode functioning with said buried word line region, said storage node, and said read bit line region as a read transistor,

wherein said body of each memory cell comprises a portion of a common substrate.

8. The dynamic random access memory as defined by claim 7 and including a conductive word line interconnecting all gate electrodes of cells along a row, and at least one conductive bit line interconnected to cells along a column.

9. The dynamic random access memory as defined by claim 8 and including switch means for selectively connecting said at least one conductive bit line to all write bit line regions in said column and to all read bit line regions in said column.

10. The dynamic random access memory as defined by claim 8 and including a write bit line connected to all write bit line regions in said column and a read bit line connected to all read bit line regions in said column.

11. A memory cell comprising

a body including a supporting substrate, a first insulating layer on said substrate, and a semiconductor layer on said first insulating layer, said semiconductor layer having a surface,

a first region of a first conductivity type in said semiconductor layer abutting said surface and electrically isolated from said substrate by said first insulating layer,

a second region of said first conductivity type in said semiconductor layer abutting said surface and spaced from said first region,

a third region of a second conductivity type in said semiconductor layer abutting said surface and positioned between and abutting said first region and said second region,

a fourth region of said second conductivity type in said semiconductor layer abutting said surface and abutting said first region opposite from said third region,

a second insulating layer on said surface, and

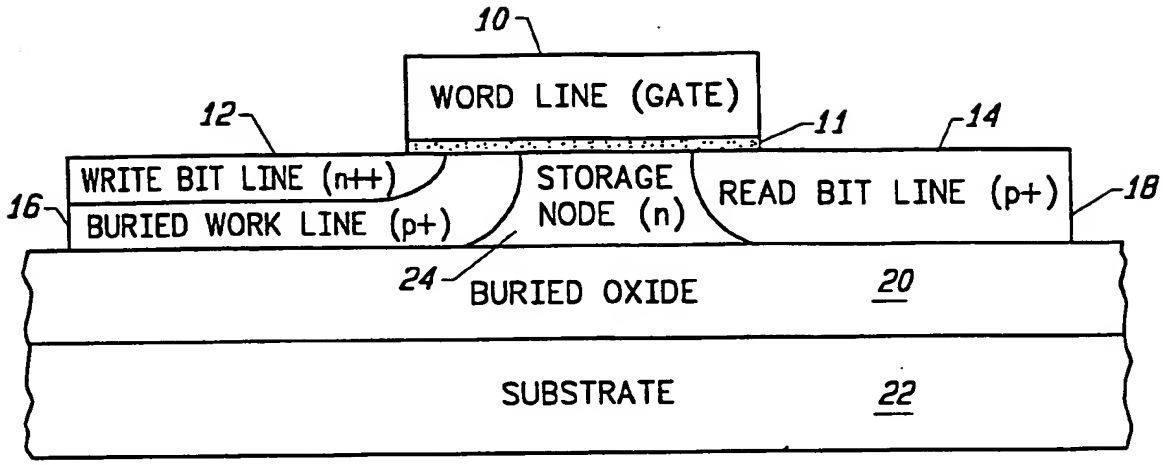
a gate electrode on said second insulating layer positioned over said first region and said third region, said gate electrode functioning with said first region, said second region and said third region as a write transistor in writing electrical charge in said first region, and said gate electrode functioning with said first region, said third region, and said fourth region as a read transistor the conductance of which is dependent on electrical charge stored in said first region.

12. The memory cell as defined by claim 11 wherein said first conductivity type is n- type and said second conductivity type is p- type.

13. The memory cell as defined by claim 12 wherein said first region is charged with a positive voltage from said second region in writing into said cell and increasing threshold voltage of said read transistor.

14. The memory cell as defined by claim 12 wherein electrons from said third region flow into said first region in writing into said cell and increasing the conductance of said read transistor.

15. The memory cell as defined by claim 11 wherein said body comprises a silicon substrate with said first insulating layer comprising silicon oxide and said semiconductor layer comprising silicon.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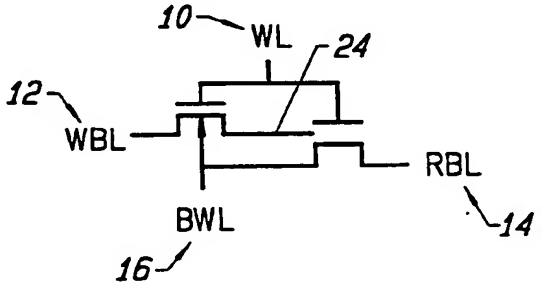
WORD LINE (GATE)
12
11
14
WRITE BIT LINE (n++)
STORAGE NODE (n)
READ BIT LINE (p+)
18
16
BURIED WORK LINE (p+)
24
BURIED OXIDE
20
SUBSTRATE
22

FIG. 1A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WL
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WBL
RBL
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BWL
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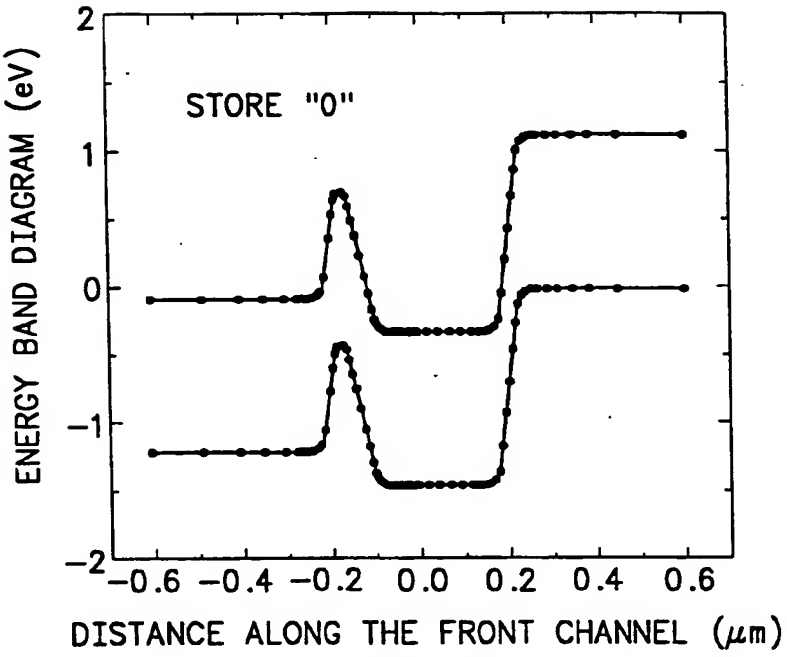
FIG. 1B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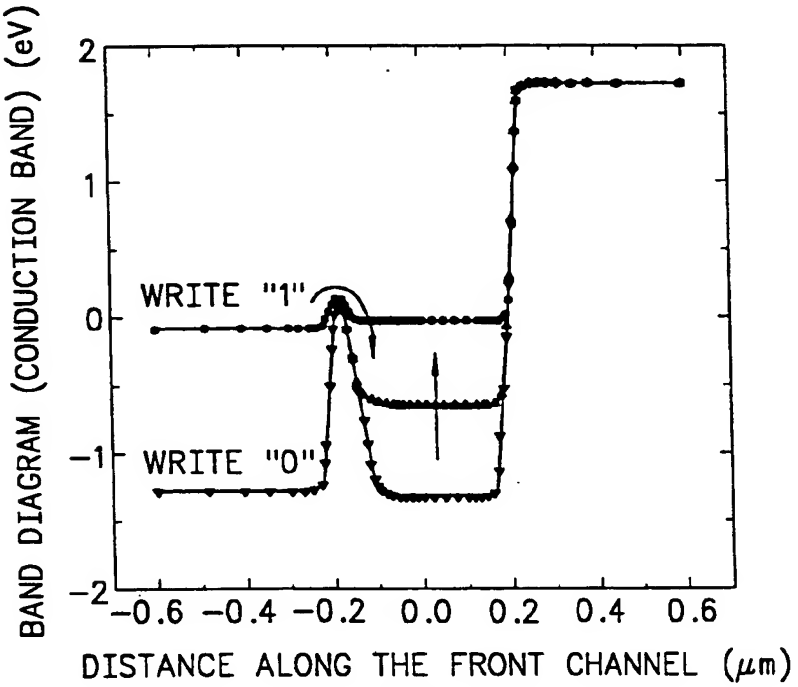
−2
−0.6 −0.4 −0.2 0.0 0.2 0.4 0.6
DISTANCE ALONG THE FRONT CHANNEL (μm)

FIG. 2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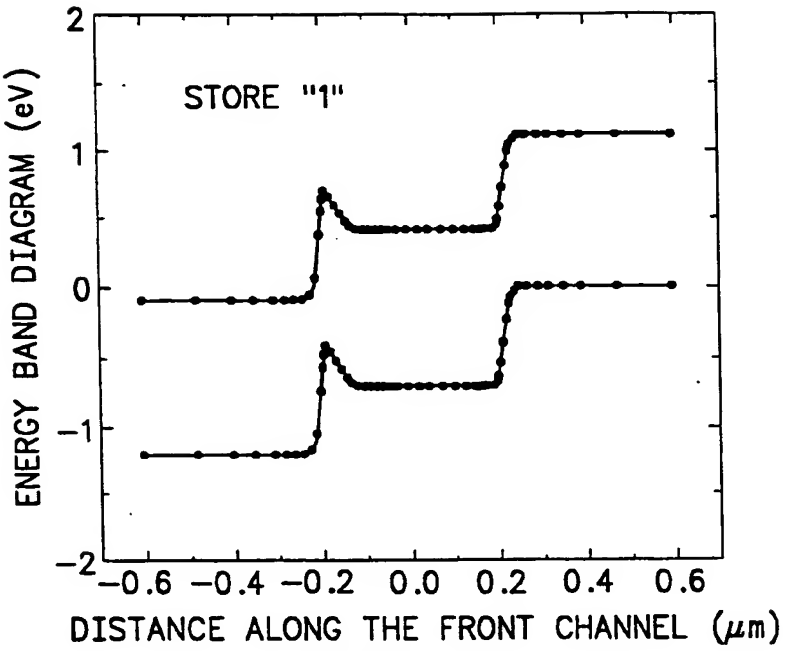
DISTANCE ALONG THE FRONT CHANNEL (μm)

FIG. 3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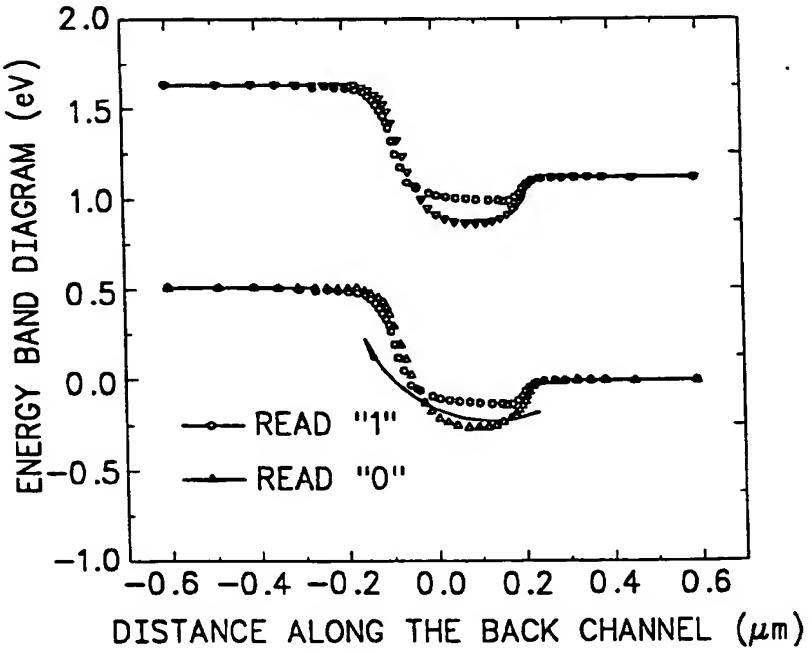
−2
−0.6 −0.4 −0.2 0.0 0.2 0.4 0.6
DISTANCE ALONG THE FRONT CHANNEL (μm)

FIG. 4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1.5
1.0
0.5
0.0
−0.5
−1.0
READ "1"
READ "0"
−0.6 −0.4 −0.2 0.0 0.2 0.4 0.6
DISTANCE ALONG THE BACK CHANNEL (μm)

FIG. 5

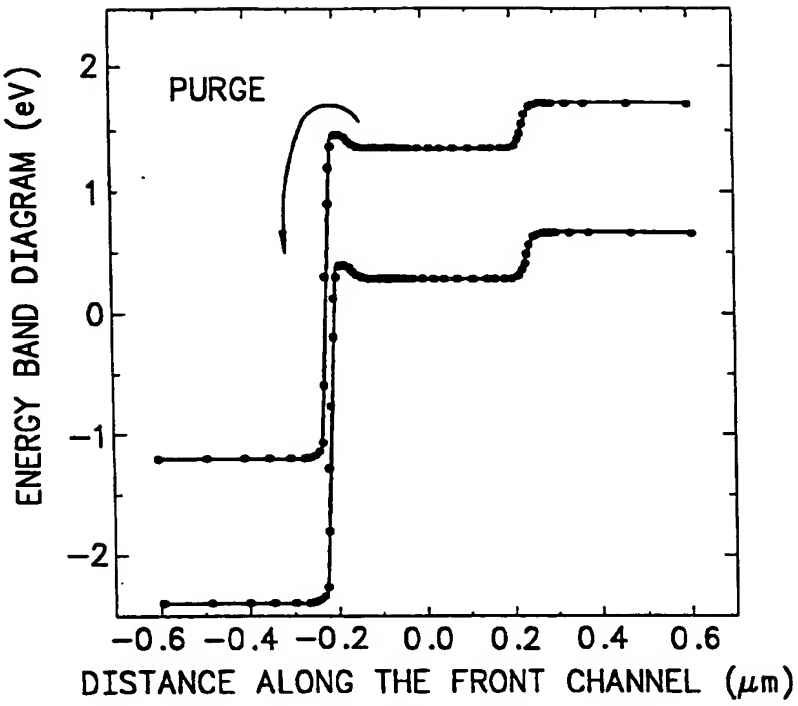
PURGE
ENERGY BAND DIAGRAM (eV)
2
1
0
−1
−2
−0.6 −0.4 −0.2 0.0 0.2 0.4 0.6
DISTANCE ALONG THE FRONT CHANNEL (μm)

FIG. 6

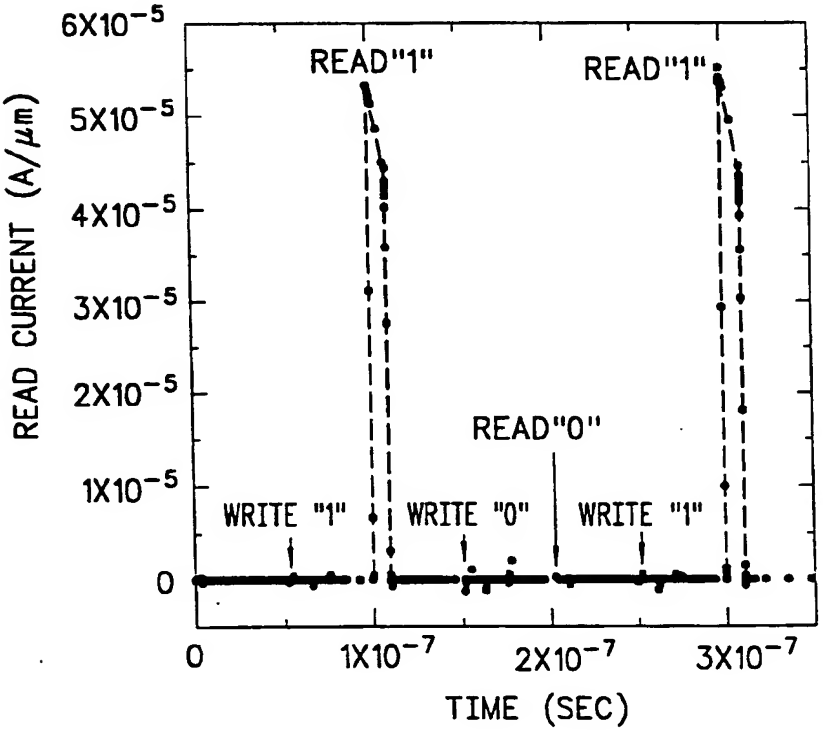
READ CURRENT (A/μm)
6X10⁻⁵
5X10⁻⁵
4X10⁻⁵
3X10⁻⁵
2X10⁻⁵
1X10⁻⁵
0
READ"1"
READ"1"
READ"0"
WRITE "1"
WRITE "0"
WRITE "1"
0
1X10⁻⁷
2X10⁻⁷
3X10⁻⁷
TIME (SEC)

FIG. 7

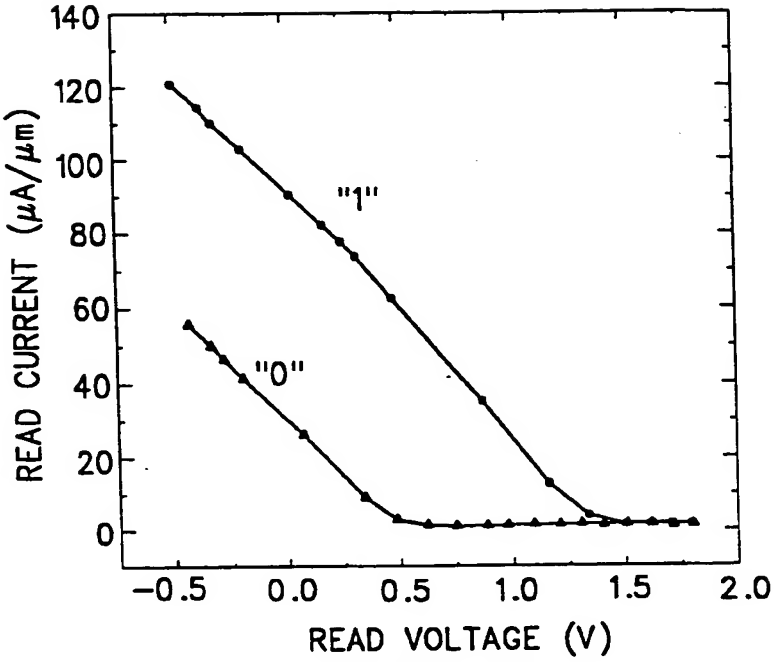
140
120
100
80
60
40
20
0
READ CURRENT (μA/μm)
"1"
"0"
−0.5
0.0
0.5
1.0
1.5
2.0
READ VOLTAGE (V)

FIG. 8

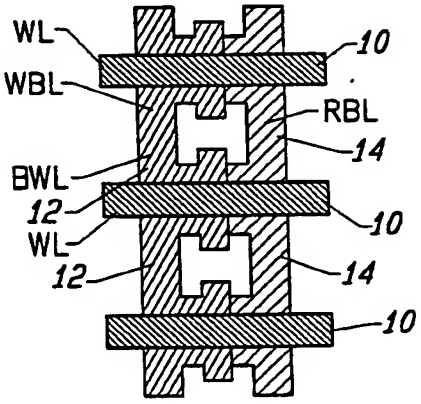
WL
10
WBL
RBL
14
BWL
12
10
WL
12
14
10

FIG. 9

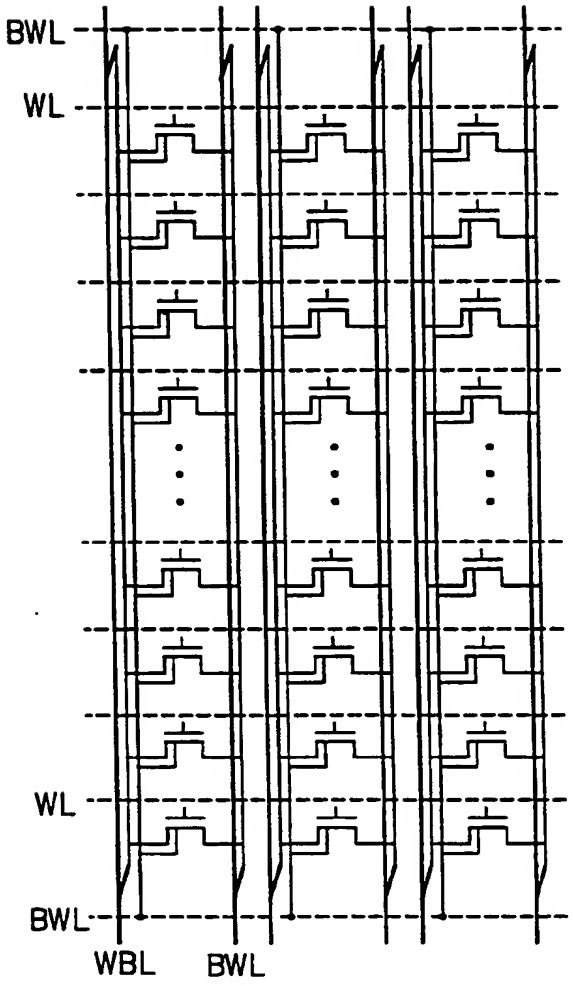

FIG. 10

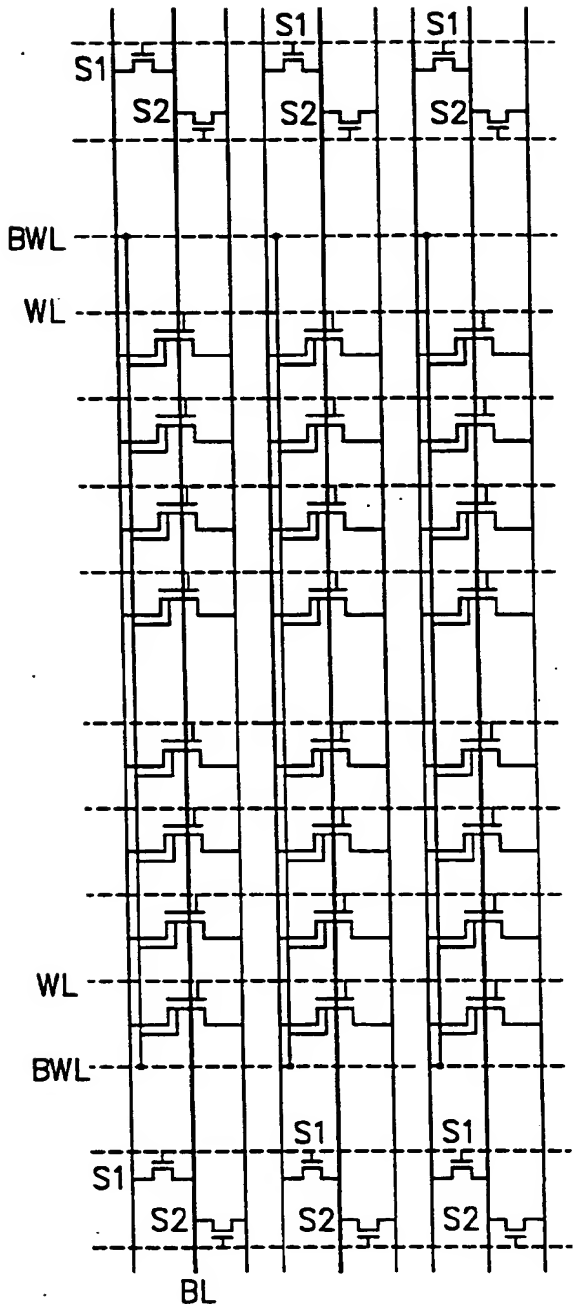

FIG. 11

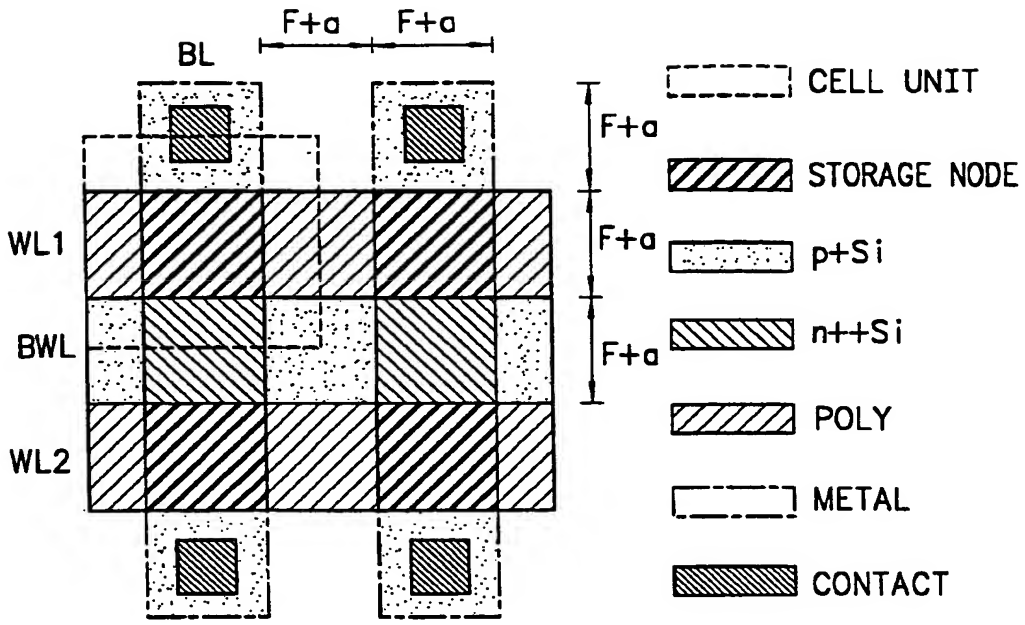
F+a
F+a
BL
WL1
BWL
WL2
F+a
F+a
F+a
CELL UNIT
STORAGE NODE
p+Si
n++Si
POLY
METAL
CONTACT

FIG. 12

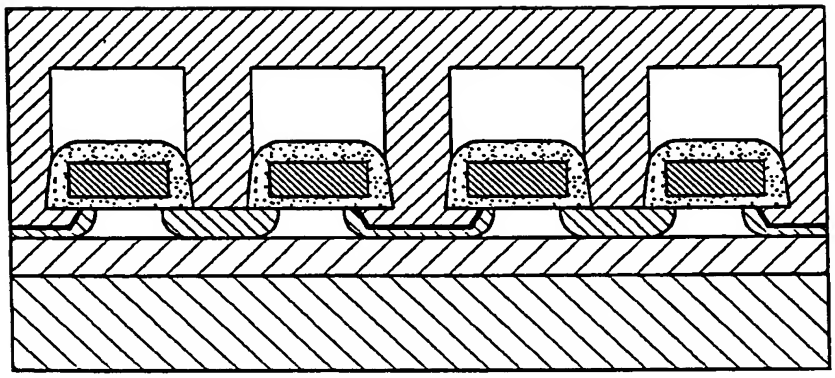

FIG. 13

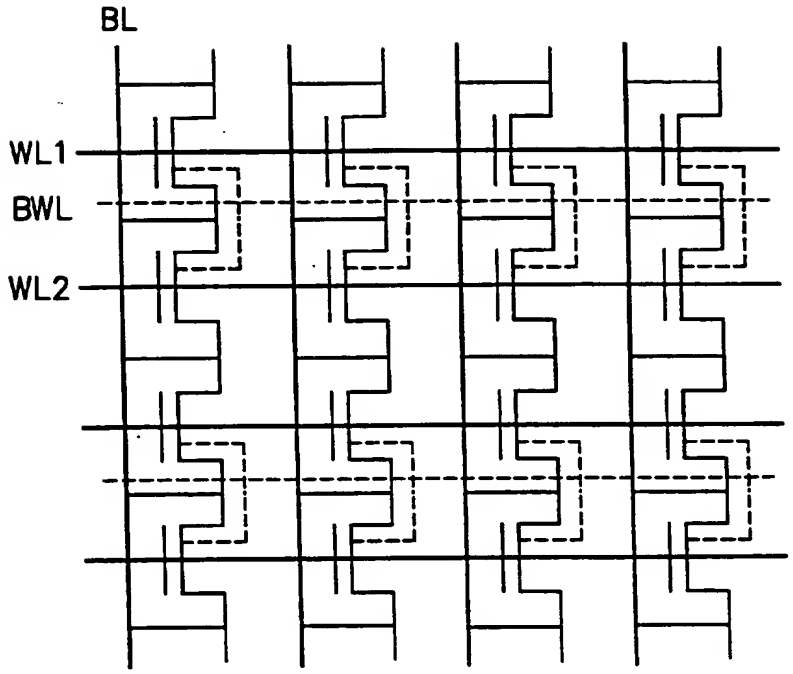

FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/13830

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :G11C 11/40
US CL :365/150,182

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 365/150,182

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4,090,254 (HO ET AL) 16 May 1978.	
X	US, A, 4,298,962 (HAMANO ET AL) 03 November 1981, col. 3, lines 55-68, and col. 6, lines 8-19.	1-15
A	US, A, 5,122,986 (LIM) 16 June 1992.	

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
20 JANUARY 1995	JAN 24 1995
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer DO HYUN YOO Telephone No. (703) 308-4908

Form PCT/ISA/210 (second sheet)(July 1992)*